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AREA EFFICIENT MEMORY REDUCED TURBO DECODING ARCHITECTURE USING NII METRIC COMPRESSION

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Abstract: The turbo codes are one of the most attactive forward error correction codes, which can privide near-optimal bit error rates(BERs) of Shannon's limit. To improve the memory in the decoding architecture a new technique namedNext Iterative Initialization (NII) metric compression technique has been introduced in our work for reducing or relaxing the turbo decoder storage demand.Since work that was done beforehand, will store all measurement esteems in this manner memory prerequisite is exceptionally high yet with regards to our proposed novel technique, it will store range of values. i.e. indexes of maximum and minimum values. The enhanced method not only decrease storage need but also provide faster response. This novel compression method will also facilitate hardware friendly recovery realization that was implemented by utilizing the simple multiplexing network.In this paper the proposed structure is designed using 4bit encoding and compared with the 8bit encoding design. Experimental results are observed by Xilinx ISE 14.5.

Keyword:Turbo Decoding, NII Metric.

I. INTRODUCTION

The turbo code presented in 1993 is one of the most impressive forward mistake adjustment channel codes, and gives close to ideal piece blunder rates(BERs), that is inside 0.5 dB ofshannon's limit at BERof 10^{-5} .Having this striking peformance, the turbo codes have honey bee accpted in many normalized versatile radio frameworks. Recently nonbinary turbo codes have have recived a grate attention and adopted in several mobile radio systems such as DVB-RCS and IEEE 8012.16 stantard (WiMAX), as they can offer numerous points of interest over the traditional single-binary turbo codes. Turbo codes are well defined in current wireless standards[2]. In 3GPP LTE-progressed particulars for an example, the unmistakable code length of 6144-bits with the code pace of 0.96[2].in request to decrease the loss of execution high code word rate disentangling, the Next Iteration Initialization (NII) technique is broadly received for the benefit of in reverse recursion instatement supplanting the system of customary sham calculation.

Though, the regular technique of Next Iteration-Initialization (NII) needs supplementary memories on behalf of storing every final backward state of on-going iteration that indicates the subsequent iteration confidence level of subsequent iteration. If the procedure of sliding window is utilized on bepicesshalf of practical realization, the number of metrics of Next Iteration-Initialization needed to be stored increases extremely with reference to window boundaries number. In order to eradicate such overhead issues, one has to adopt novel idea, the procedure called static compression scheme will resolve such overhead problems by providing transfer function of dedicated to encoding the next iterative initialization metric into three or four bits.Simultaneously, the most developed examination will likewise encourage the dynamic scaling for the benefit of encoding the Next Iteration Initialization (NII) measurements. But past procedures need large quantity of storage bits because of every state metrics need to be collected after a specific process of compression.

II. PREVIOUS WORKS

A. Conventional Turbo Decoding Architecture

Figure.1. is the generalized architecture of turbo decoding with reference of soft-input soft-output decoders. In this decoder, the decoding will have done in two phases

1 In-order phase

2 Interleaved phase

Here within the Figure 1, the sequence of input Log-likelihood Ratio (LLR) of bits of systematic as well as the parity bits are indicated as Λ_s (or Λ_s^I) &Λ_{p1} (or Λ_{p2}^I), respectively. Here within this symbol the superscript I indicate the order of sequence associated to interleaved phase with reference to the Log likelihood Ratio (LLR) as well as the priori information. i.e. Information of extrinsic Λ_e (or Λ_e^I), which will be opposite phase priori information after getting into interleaver (or else de-interleaver).Inside these two stages, they are restrictive in time, just a single delicate in delicate out decoder is acknowledged inside training for the benefit of understanding the cycle of time-interleaved.

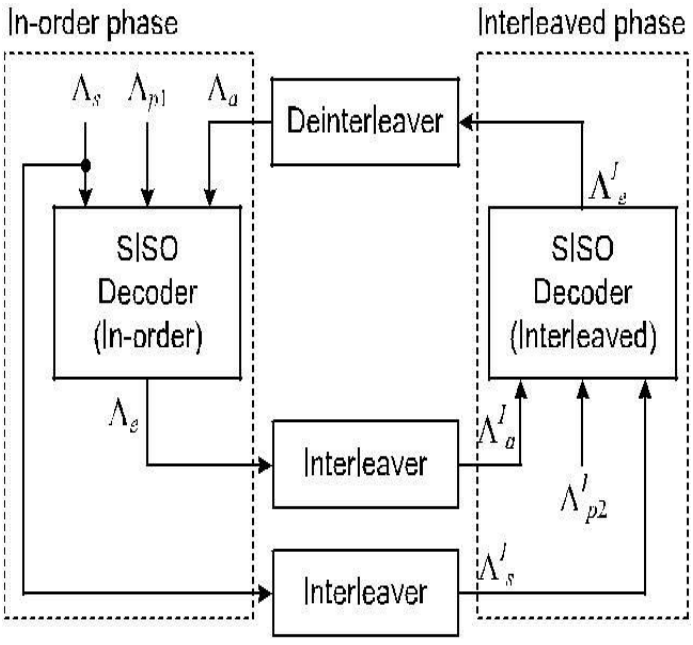

Figure 1:CONVENTIONALTURBO DECODING ARCHITECTURE

B. Technique of Sliding-Window with NII metric compression

For turbo decoders, the method of sliding window has been generally embraced so as to decrease the interior cushion size[6] Exhibit the strategy of interpreting for the benefit of n-bit codeword aligned with w-bits sliding window. Figure 2.Show the method of interpreting for n-cycle codeword aligned with w-bits sliding window.Regarding the calculation of Maximuma-posteriori (MAP) disentangling, each sliding must handle state metric recursively with bearing of forward by using the resulting branch measurement. On behalf of reliability, i^{th} trellis corresponding kth forward metrics entitled as

$\alpha_i(0)$, $\alpha_i(1)$, … . , $\alpha_i(k-1)$.Inside the regressive recursion that will cycle each lattice outward data just as the resulting state metric inside reverse way. As alike of state metric of forward, i^{th} trellis corresponding backward metric represented as

$\beta_i(0)$, $\beta_i(1)$, $\beta_i(2)$, $\beta_i(3)$ … … $\beta_i(k-1)$. As earlier of commencing the backward recursion, it is very essential to initialize properly the initial confidence level of every backward state.

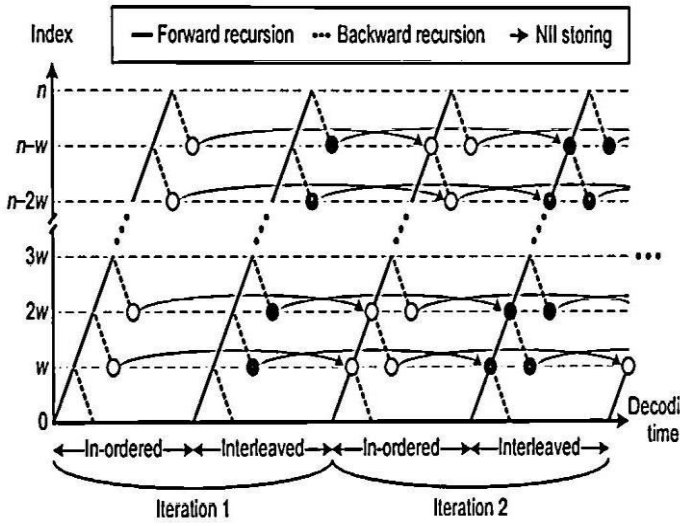

Figure 2:SLIDING-WINDOW-BASED TURBO DECODING WITH NII TECHNIQUE

The encoding function for the 3- bit encoding is depicated in fig. 3(a). The encoding function for the 4-bit encoding can be similary defined. Possible vales at the border are listed in table I. As the range of the orignal border mertics is [-512,+511] which can be represented with 10 bits the proposed border metric encoding can be obtained by limiting the value into [-256,+256] for the 4-bit encoding and [-64,+64] for the 3- bit encoding and by allowed only power- of-two values.

Each Metric of next cycle introduction must be contrasted and the reference esteem, however that requires the various assessments as appeared in figure 3(b). in more precisely every state metric must be assessed with the estimations of six reference levels just as the assessment esteems are used for the benefit of creating the 3-digit pressure metric of NII are perused from the memory of NII and nursed into the organization of recuperation to reproduce the retrogressive recursion beginning values.Similar to the advance work was done in late time dynamic calculation in the interest of each NII metric[8]. However, it needs the various stockpiling pieces and gear of equipment to encourage the worthy exhibition of touch mistake rate, which expend more force. Here noted one is past work is regarding free pressure of each state metric. As each k-1 real state metric must be encoded just as put away inside the memory of NII metric, the diminished inside the memory pieces is confined by the nature. Simultaneously, the calculation which was proposed will consider the scope of estimations of NII metric to make putting away information in solid arrangement.

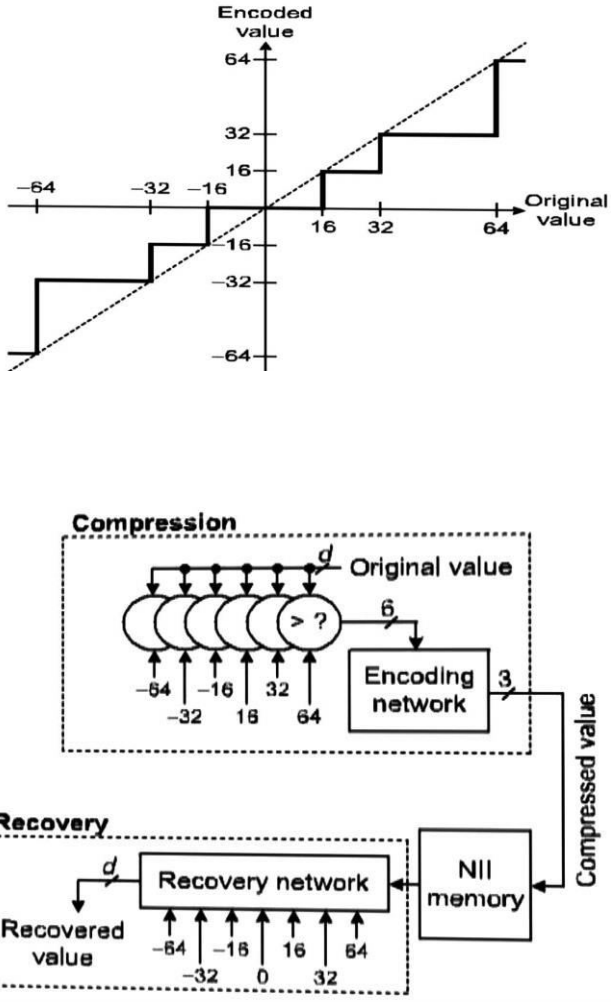

Figure 3:(a) 3-BIT BORDER METRIC ENCODING FUNCTION

(b) ENCODING AND DECODING

TABLE I

ENCODED VALUES FOR BORDER METRICS

Encoding Scheme	Encoded vales for border metric
4- bit encoding	±256,±128,±64,±32,±16,±8,±4,0
3-bit encoding	±64,±32,±16,0

III. Proposed NII Metric Compression Model

As the best log-MAP unraveling just bright lights on the cross section way expending the best relentlessness, it is

basic to pick the most solid state at the instating system of every window. In no way like the previous works protecting each state metric persuading power in any case much as could be typical, the extended NII metric weight considers the degree of state estimations implied as Δx, i.e., the alteration between the most outrageous and slightest state regards among the wxth in invert state estimations, βwx(•).It is conceivable to make the touch width of Δx more minute submersion of accomplishes beating a specific respect is elegant without debasing the BER execution [9]. In perspective of the different proliferations, only 8 bits are adequate to address Δx, while each one of a kind state metric requires in any occasion more than 12 bits to neutralize surges in the LTEimpelled structures .To give an understanding for the assurance levels of each state at the recovery technique, in addition, we store the records of the most outrageous and slightest states, addressed as IMAX x and IMIN x, separately.

Adroitly, the proposed weight framework tries to offer the right data of the zenith separates by surrendering the accuracy of each state assessments, while the previous works essentially think about the approximations of each state metric. Augmentation results, display that the BER of the proposed work utilizing accurate Δx is essentially indistinct to those of the past NII metric encoding plans. In this manner, the proposed assessment decreases the measure of breaking point bits essentially without debasing the spoil evolving limit. Right when the level of a sliding window is set to 32, for the event of 6144 bits turbo codes, our weight think up utilizes just 5376 bits for NII data, which is multiple times not as much as the standard assessment. Like the previous works, the proposed NII metric weight correspondingly requires extra calculations for the encoding and unraveling shapes.

In the proposed weight, as exemplified in Fig.4 regulating eight thus around states suggested as βwx(•), the measure of assessments can be phenomenally decreased by sharing the temporary outcomes. To discover Δx proficiently, three essential modules are used in the proposed planning. The SUB/CLIP unit calculates the last yield Δx with the decreased piece width d.

It is striking that IMAX x and IMIN x can be easily made by social event the prior examination results. Note that it is hard to diminish the amount of examinations at the past estimation as most of the pressing structures are self-sufficient of each other.

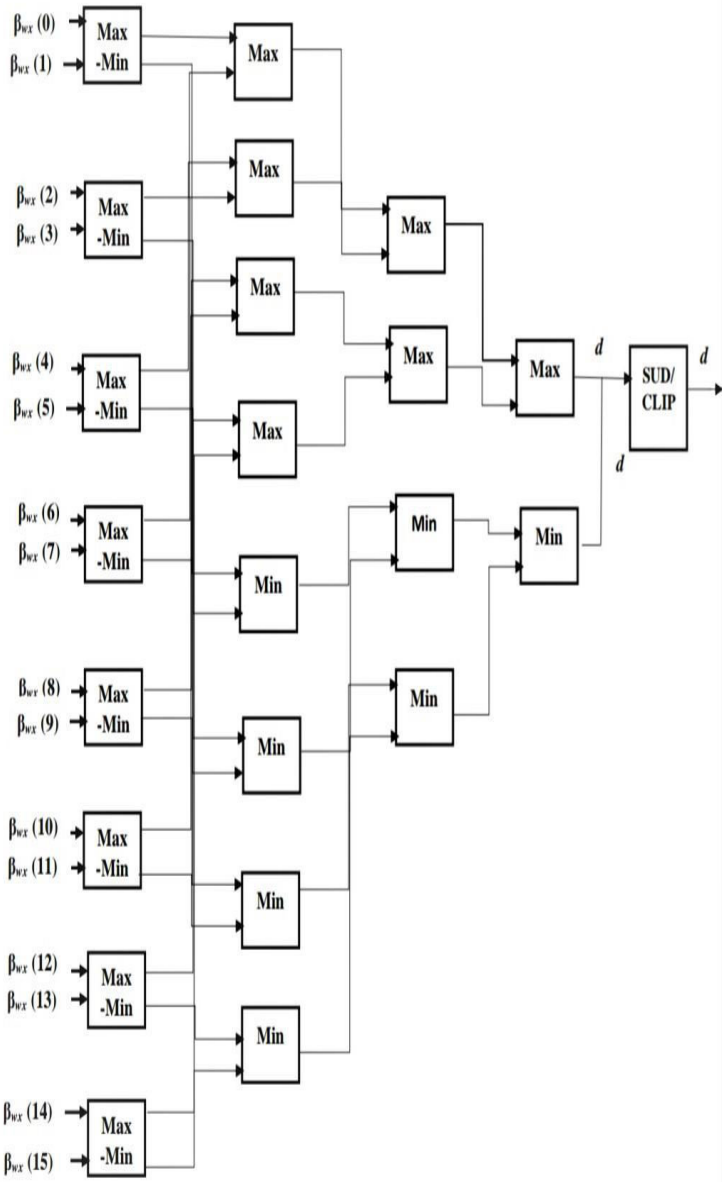

Figure 4:SIXTEEN STATE METRIC BASED ON THE PROPOSED NII METRIC COMPRESS

IV. EXPERIMENTAL RESULTS

Result of the proposed design is implemented using Xilinx ISE for simulation and Synthesis

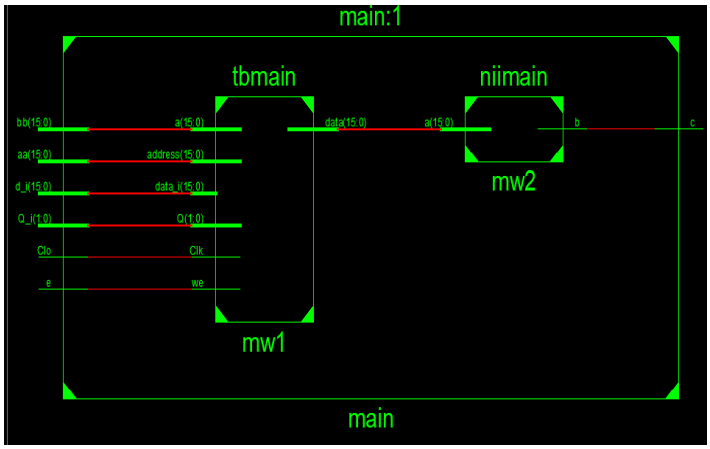

Figure 5:IMPLEMENTED SCHEMATIC BLOCK

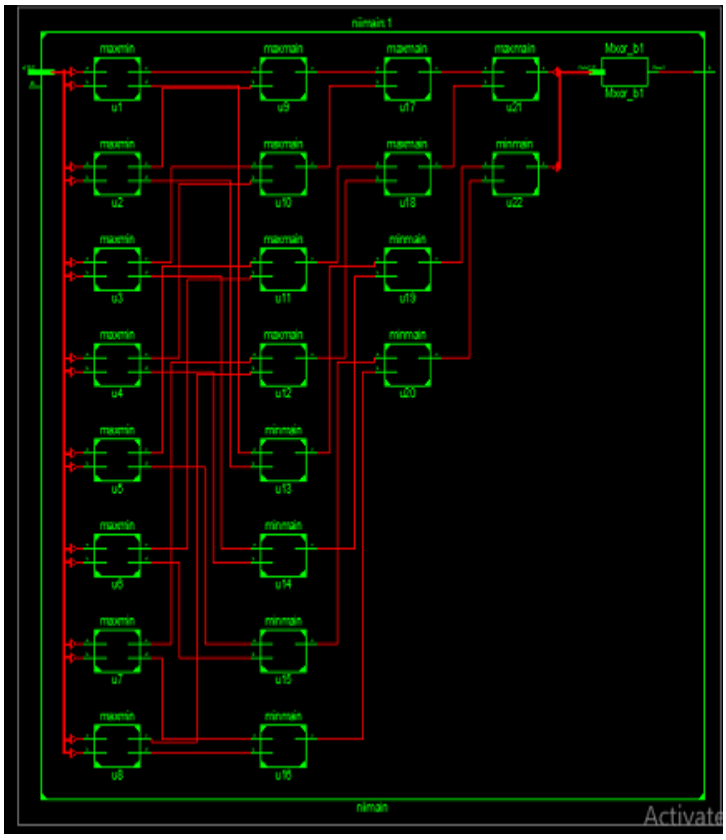

Figure 6:RTL SCHEMATIC OF NII METRIC

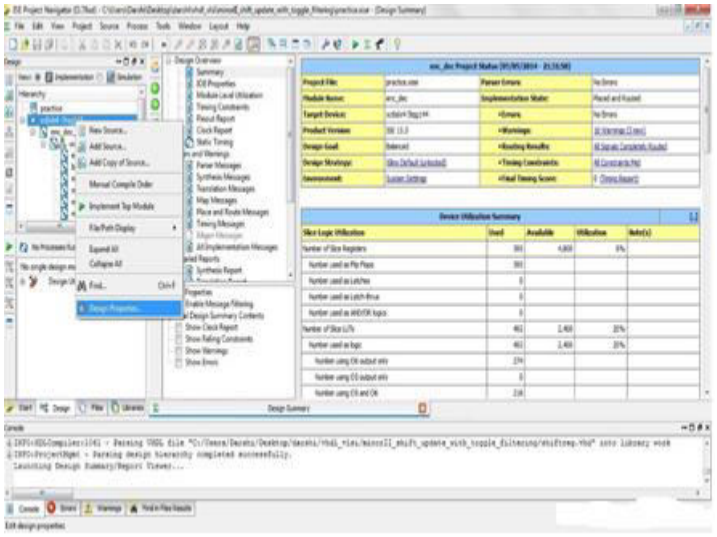

Figure 7:DESIGN SUMMARY

```
Data Path: m4/m4/ct/cnt_m1_0 to out<63>
                                   Gate     Net
  Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   FDRSE:C->Q           13   0.514   0.836  m4/m4/ct/cnt_m1_0 (m4/m4/ct/cnt_m1_0)
   RAM16X1D:DPRA0->DPO   1   0.612   0.387  m4/m4/ct/Mram_d_middle3 (m4/m4/ct/_varindex0002<
   LUT4:I2->O            1   0.612   0.357  m4/m4/ct/out<2>1 (out_62_OBUF)
   OBUF:I->O                 3.169          out_62_OBUF (out<62>)
  ----------------------------------------
  Total                      6.487ns (4.907ns logic, 1.580ns route)
                                     (75.6% logic, 24.4% route)

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Total REAL time to Xst completion: 68.00 secs
Total CPU time to Xst completion: 68.42 secs

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Figure 8:TIMING SUMMARY

TABLE II COMPRESSION TABLE

Desing	Area			Delay(ns)
	Slices	Flip Flops	LUTs	
Existing System	4543	6064	6337	6487
Proposed System	53726	61745	63400	6487

V. CONCLUSION

The proposed design could reach the memory demands of turbo decoders. By storing the precise ranges rather than the individually compressed metrics, the proposed calculation amazingly lessens the size of NII metric memory while accomplishing an appealing blunder adjusting error-correcting capability. Simulation and Synthesis is observed by Xilinx.

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